UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P O Box 1450
Alexandria, Virginia 22313-1450
www uspto gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,899	12/16/2003	Atsuhiro Otaka	032172	5713

38834 7590 05/12/2009
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
TRUONG, LOAN	

ART UNIT	PAPER NUMBER
2114	

MAIL DATE	DELIVERY MODE
05/12/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,899	OTAKA ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-10,15-18,23-28,32 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-10,15-18,23-28,32 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to applicant's arguments filed on January 30, 2009 in application #10/735,899.

2. Claims 5-10, 15-18, 23-28 and 32-33 are presented for examination. Claims 1-4, 11-14, 19-22 and 29-31 are cancelled. Claims 5-6, 8-10, 15-18, 23-26 and 32-33 are amended.

Response to Arguments

3. Applicant's arguments, filed January 30, 2009, with respect to the rejection(s) of claim(s) 5-10, 15-18, 23-28 and 32-33 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Miller US 6,308,265.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 5-10, 15-18, 23-28 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Angelo et al. (US 7,073,064) in further view of Miller (US 6,308,265).

In regard to claim 5, Angelo et al. does not teach the redundancy management method for BIOS according to claim 7, further comprising a step of preventing switching of said memory in standby to said memory in operation when the update of said BIOS in said memory in standby failed.

> Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region (*col. 6 lines 1-10*). The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process (*col. 7 lines 45-62*).
>
> Refer to claim 7 for motivational statement.

In regard to claim 6, Angelo et al. does not teach the redundancy management method for BIOS according to claim 7, further comprising a step of preventing switching said memory

switched to standby, to said memory in operation when writing of said BIOS in said memory switched to standby failed.

Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region (*col. 6 lines 1-10).* The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process (*col. 7 lines 45-62).*

Refer to claim 7 for motivational statement.

In regard to claim 7, Angelo et al. teach a redundancy manager method for BIOS, comprising the steps of:

using one of a pair of memories (*two separately programmable portions, col. 1 lines 47-49)*, which respectively store the BIOS for setting hardware in an environment in which OS can use said hardware, for operation and the other standby (*each contain identical copies of the BIOS software with an active and inactive portion, col. 1 lines 48-52)*;

executing an update of said BIOS by writing to said memory in standby (*to update the BIOS, the inactive half is overwritten first, col. 1 lines 50-54)*;

permitting switching said memory in standby to in operation when the update of said BIOS in said memory in standby succeeded (*once the system is power cycled the second time,*

the system is brought up with the newly portion of the BIOS being active, the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56);

switching said permitted memory in standby in operation, and said memory in operation to in standby when said hardware is started up (*system is brought up with the newly overwritten portion of the BIOS being active, col. 1 lines 47-56).*

Angelo et al. does not teach the method for BIOS comprising the steps of: switching to the BIOS in said memory in standby when the BIOS in said one memory cannot be booted; and preventing execution of said switching when said hardware is started up for power recovery.

Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region (*col. 6 lines 1-10).* The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process (*col. 7 lines 45-62).*

It would have been obvious to modify the method of Angelo et al. by adding Miller protection of boot block code. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide protection for boot block code used to boot up a computer (*col. 3 lines 52-63).*

In regard to claim 8, Angelo et al. does not teach the redundancy management method for BIOS according to claim 7, further comprising a step of preventing execution of said redundancy step when said hardware is started up for power recovery.

> Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region (*col. 6 lines 1-10*). The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process (*col. 7 lines 45-62*).
>
> Refer to claim 7 for motivational statement.

In regard to claim 9, Angelo et al. does not teach the redundancy management method for BIOS according to claim 7, further comprising a step of executing the update of BIOS in a memory in standby of another hardware connected with said hardware according to the update of the BIOS in said memory in standby of said hardware.

> Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing an updatable part of the BIOS (*col. 5 lines 11-16*) to update the BIOS image while protecting the boot block code (*col. 5 lines 26-32*).
>
> Refer to claim 7 for motivational statement.

In regard to claim 10, Angelo et al. does not teach the redundancy management method for BIOS according to claim 7, further comprising a step of executing the synchronization processing of the BIOS with another hardware connected with said hardware.

Miller teaches the protection of boot block code by implementing a match of boot block code in another region of the flash part (*abstract).*

Refer to claim 7 for motivational statement.

In regard to claim 15, Angelo et al. does not teach the data processing apparatus according to claim 27, wherein said CPU prevents switching said memory in standby to the memory in operation when the update of said BIOS in said memory in standby failed.

Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region (*col. 6 lines 1-10).* The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process (*col. 7 lines 45-62).*

Refer to claim 7 for motivational statement.

In regard to claim 16, Angelo et al. does not teach the data processing apparatus according to claim 27, wherein said CPU prevents switching said memory switched to standby, to said memory in operation when writing of said BIOS in said memory switched to standby failed.

> Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region (*col. 6 lines 1-10).* The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process (*col. 7 lines 45-62).*
>
> Refer to claim 7 for motivational statement.

In regard to claim 17, Angelo et al. does not teach the data processing apparatus according to claim 27, further comprising another hardware connected with said hardware, and said hardware executes the update of the BIOS in the memory in standby of said other hardware connected with said hardware according to the update of the BIOS in said memory in standby of said hardware.

> Miller teaches the first region, in which the boot block code is stored, is copied to another region (*fig. 3, col. 5 lines 44-49).*
>
> Refer to claim 7 for motivational statement.

In regard to claim 18, Angelo et al. teach the data processing apparatus according to claim 11, wherein said hardware executes the synchronization processing of the BIOS with said other hardware connected with said hardware.

Miller teaches the first region, in which the boot block code is stored, is copied to another region *(fig. 3, col. 5 lines 44-49)* and the boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process *(col. 7 lines 45-62).*

Refer to claim 7 for motivational statement.

In regard to claim 23, Angelo et al. teach the storage system according to claim 28, wherein said CPU of said storage control apparatus prevents switching said memory in standby to the memory in operation when the update of said BIOS in said memory in standby failed.

Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region *(col. 6 lines 1-10).* The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process *(col. 7 lines 45-62).*

Refer to claim 7 for motivational statement.

In regard to claim 24, Angelo et al. does not teach the storage system according to claim 24, wherein said CPU of said storage control apparatus prevents switching said memory switched to standby, to said memory in operation, when writing of said BIOS in said memory switched to standby failed.

Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region *(col. 6 lines 1-10)*. The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process *(col. 7 lines 45-62)*.

Refer to claim 7 for motivational statement.

In regard to claim 25, Angelo et al. teach the storage system according to claim 28, further comprising another storage control apparatus, which is connected to said storage devices and said storage control apparatus and for controlling said storage devices, wherein said storage control apparatus executes the update of the BIOS in the memory in standby of said other storage control apparatus according to the update of the BIOS in said memory in standby of said storage control apparatus.

Miller teaches the first region, in which the boot block code is stored, is copied to another region *(fig. 3, col. 5 lines 44-49).*

Refer to claim 7 for motivational statement.

In regard to claim 26, Angelo et al. teach the storage system according to claim 28, further comprising another storage control apparatus, which is connected to said storage devices and said storage control apparatus and for controlling said storage devices, wherein said storage control apparatus executes the synchronization processing of the BIOS with said other storage control apparatus.

Miller teaches the first region, in which the boot block code is stored, is copied to another region *(fig. 3, col. 5 lines 44-49)* and the boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process *(col. 7 lines 45-62).*

Refer to claim 7 for motivational statement.

In regard to claim 27, Angelo et al. disclosed a data processing apparatus, comprising:

a hardware including a CPU *(fig. 3, 200)*;

a pair of memories *(two separately programmable portions, col. 1 lines 47-49)* which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware *(each contain identical copies of the BIOS software with an active and inactive portion, col. 1 lines 48-52)*; and

wherein said CPU executes the update of said BIOS after a successful boot-up by writing to said memory in standby (*to update the BIOS, the inactive half is overwritten first, col. 1 lines 50-54)*,

wherein said service processor permits switching said memory in standby to said memory in operation when the update of said BIOS in said memory in standby succeeded (*once the system is power cycled the second time, the system is brought up with the newly portion of the BIOS being active, the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56)*,

wherein said service processor switches said permitted memory in standby to a memory in operation, and said memory in operation to said memory in standby when said hardware is started up (*system is brought up with the newly overwritten portion of the BIOS being active, col. 1 lines 47-56)*.

Angelo et al. does not teach a data processing apparatus, comprising of a service processor for using one of said pair of memories for operation and the other for standby when said hardware is started up and switching to the BIOS in said memory in standby when the BIOS of said one memory cannot be booted and wherein said CPU prevents execution of said switching when said hardware is started up for power recovery.

Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region (*col. 6 lines 1-10)*. The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved

even when a power down occurs and maintained in the same state to provide correct execution of a booting process (*col. 7 lines 45-62).*

Refer to claim 7 for motivational statement.

In regard to claim 28, Angelo et al. teach a storage system, comprising:

a storage control apparatus comprises:

a hardware including a CPU (*fig. 3, 200)*;

a pair of memories (*two separately programmable portions, col. 1 lines 47-49)* which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware (*each contain identical copies of the BIOS software with an active and inactive portion, col. 1 lines 48-52)*; and

a plurality of storage devices connected to said storage control device,

wherein said CPU of said storage control apparatus executes the update of said BIOS by writing to said memory in standby (*to update the BIOS, the inactive half is overwritten first, col. 1 lines 50-54),*

wherein said service processor of said storage control apparatus permits the switching of said memory in standby to said memory in operation when the update of said BIOS in said memory in standby succeeded (*once the system is power cycled the second time, the system is brought up with the newly portion of the BIOS being active, the older BIOS routine can be updated while it is inactive, col. 1 lines 52-56),*

wherein said service processor of said storage control apparatus switches said permitted memory in standby to a memory in operation, and said memory in operation to said memory in

standby when said hardware is started up (*system is brought up with the newly overwritten portion of the BIOS being active, col. 1 lines 47-56).*

Angelo et al. does not teach a storage system comprising: a service processor for using one of said pair of memories for operation and the other for standby when said hardware is started up and switching to the BIOS in said memory in standby when the BIOS of said one memory cannot be booted, and wherein said CPU prevents execution of said switching when said hardware is started up for power recovery.

Miller teaches the protection of boot block code while allowing write accesses to the boot block by implementing boot-block-in-progress flag indicating that an updating of the BIOS is being performed wherein if a power failure occurs the flag, bit, would still be in the set state and CPU will boot the PC from the backup boot block image in the second region and not from the boot block image in the first region (*col. 6 lines 1-10).* The boot block-in-progress flag is configured in a 2:1 switch where the value is preserved even when a power down occurs and maintained in the same state to provide correct execution of a booting process (*col. 7 lines 45-62).*

Refer to claim 7 for motivational statement.

In regard to claim 32, Angelo et al. teach the redundancy management method for BIOS according to claim 7, further comprising writing the BIOS of said one memory switched to operation, to said the other memory switched to standby for redundancy after said switching and successful booting up of said BIOS of said one memory switched to operation when a version of the BIOS of said other memory is different from a version of said BIOS of said one memory

(*once the system is brought up with the newly overwritten portion of the BIOS being active, the section containing the older BIOS routine can be updated while it is inactive, col. 1 lines 47-63).*

In regard to claim 33, Angelo et al. teach the data processing apparatus according to claim 27, wherein said writing comprising writing the BIOS of said one memory switched to operation, to said the other memory switched to standby for redundancy after said switching and successful booting up of said BIOS of said one memory switched to operation when a version of the BIOS of said other memory is different from a version of said BIOS of said one memory (*once the system is brought up with the newly overwritten portion of the BIOS being active, the section containing the older BIOS routine can be updated while it is inactive, col. 1 lines 47-63).*

****

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 10am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
AU 2114

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114